Effect of Reduced Graphene Oxide Cap Layer on Electromigration Reliability of Cu Interconnect

Seong Jun Yoon, Sung-Yool Choi, and Byung Jin Cho

Department of Electrical Engineering, KAIST, 291 Daehak-Ro, Yuseong-gu, Daejeon 305-701, Korea
elebjcho81@kaist.ac.kr

As the interconnect size have been scaled down, electromigration (EM) becomes one of the major issues of Cu interconnect reliability. In the typical Cu damascene structure, the location of Cu and Si(C)N dielectric layer interface is the weakest point of electromigration-induced failure. Therefore, introducing metallic cap layer, such as tungsten [1] or CoWP [2], could effectively increase the EM lifetime of Cu interconnect. However, difficulty in process optimization and cost efficiency become major barriers [3]. Moreover, as the Cu line width reduces, ultra-thin cap layer with high EM blocking ability is necessary. Graphene-based 2-D materials, which have atomically thin nature, could have strong potential to application of Cu interconnect cap layer. In this work, we investigate that a reduced graphene oxide (rGO) cap layer effectively blocks the migration path of Cu surface, and therefore, the EM lifetime of Cu line is improved. The rGO cap layer was fabricated by dip-coating of water-dispersible graphene oxide solution and subsequent reduction with hydrogen ambient annealing. The electromigration test was conducted under highly accelerated wafer level test and the mean temperature of the Cu line was estimated [4]. The EM test results indicate the major diffusion mechanism of Cu atom is changed from surface diffusion to grain boundary diffusion, because of the EM blocking by rGO cap layer. The Observation of Cu line morphology by scanning electron microscopy also support the result of increased EM lifetime by rGO cap. A possible mechanism for reduced surface diffusivity of Cu line is also proposed.

References

[1] T. Saito et al., IEEE Trans. Electron Devices, **51** (2004), 2129.
[2] C.-K. Hu et al., Microelectron. Eng., **70** (2003), 406.
[3] C.-C. Yang et al., IEEE Electron Device Lett., **31** (2010), 728.
[4] A. Zitzelsberger et al., Proc. Int. Reliability Physics Symp., (2003), 161.

Figures

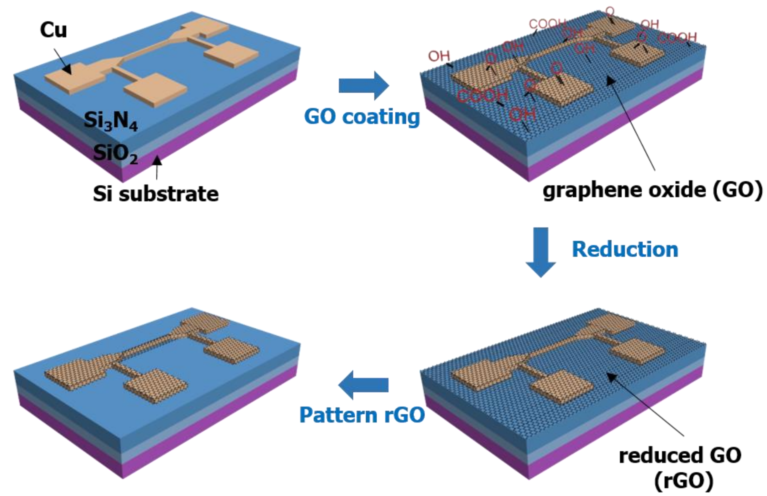

Figure 1. Fabrication process of rGO cap layer on Cu line